REMARKS

In the outstanding Office Action, the Examiner rejected claims 1-2 and 4-20 of the present invention on reference grounds. Specifically, the Examiner rejected:

claims 1-2, 4, 6-7, 9 and 11-16 under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 6,069,398 to Kadosh et al. (hereinafter "Kadosh");

claims 17-19 under 35 U.S.C. § 102(b) as allegedly anticipated by Kadosh;

claims 5 and 20 under 35 U.S.C. § 103(a) as allegedly obvious over Kadosh;

claim 8 under 35 U.S.C. § 103(a) as allegedly obvious over the combination of Kadosh and U.S. Patent No. 6,027,964 to Gardner et al. (hereinafter "Gardner"); and

claim 10 under 35 U.S.C. § 103(a) as allegedly obvious over the combination of Kadosh and U.S. Patent No. 6,436,747 to Segawa et al. (hereinafter "Segawa").

Applicants respectfully traverse the Examiner's rejections of claims 1-2 and 4-20, for the following reasons:

Claim 1, from which claims 2 and 4-16 depend, positively recites formation of "**a protective dielectric layer overlying said polysilicon layer in said at least one polysilicon resistor device region**." Similarly, claim 17, from which claims 18-20 depend, has been amended to positively recited deposition of "**a protective layer over the polysilicon layer of the polysilicon resistor**."

The Examiner asserted in the outstanding Office Action that the Kadosh reference discloses a protective dielectric layer 130 that covers a polysilicon layer in a polysilicon resistor device region (see Office Action, page 3, lines 5-6), referring to column 8, lines 41-44 and Figure 2E of Kadosh.

However, column 8, lines 41-44 and Figure 2E of Kadosh disclose the formation of a blanket intralayer dielectric (ILD) layer 130 over a polysilicon gate 104, which is a part of the N-channel transistor 110, but the polysilicon gate 104 is **not located in** a polysilicon resistor device region; nor does the polysilicon gate form **a part of** the polysilicon resistor 136. In other words, the polysilicon gate 104 as disclosed by Kadosh does not constitute a polysilicon layer "**in** [said] at least one polysilicon resistor device region," as positively recited by claims 1-2 and 4-16 of the present application, or a polysilicon layer "**of** the polysilicon resistor," as positively recited by claims 17-20 of the present application. Although Kadosh does disclose a polysilicon resistor 136 that contains a polysilicon layer (see Kadosh, column 9, lines 53-59 and Figures 2H and 2I), the blanket intralayer dielectric (ILD) layer 130 is located **under** (instead of over) the polysilicon resistor 136.

The Examiner's assertion that Kadosh discloses a protective dielectric layer 130 that covers a polysilicon layer in a polysilicon resistor device region therefore contradicts with the actual disclosure of Kadosh.

As a matter of fact, Kadosh fails to provide any derivative basis for a protective dielectric layer that overlays a polysilicon layer of at least one polysilicon resistor device region or for a protective layer that is located over a polysilicon layer of a polysilicon resistor, as positively recited by claims 1-2 and 4-20 of the present application.

Gardner discloses a diffused resistor that is formed by doping a resistor region 104 in a silicon substrate (see Gardner, Figure 1B, and column 6, lines 26-28). **Nothing in Gardner teaches or suggests formation of a polysilicon layer in the resistor region 104**, much less a protective dielectric layer that overlays a polysilicon layer in at least one polysilicon resistor device region or a protective layer that is located over a polysilicon layer of a polysilicon resistor.

Therefore, Gardner cannot remedy the above-described deficiency of Kadosh.

Segawa discloses formation of a TEOS film 10 over a polysilicon resistor 13 (see Segawa, Figure 3a). The TEOS film 10 of Segawa is formed **after** a resistance value has been provided

to the polysilicon resistor 13 by masked implantation of dopant ions into the polysilicon resistor 13 (see Segawa, Figures 2b-3a).

In contrast, claims 1-2 and 4-16 of the present application positively recites formation of the protective dielectric layer **before** a predetermined resistance value is provided to the polysilicon layer in the at least one polysilicon resistor device region, and claims 17-20 positively recites ion implantation into the polysilicon layer in the polysilicon resistor **through the protective layer**.

Therefore, a combination of the Kadosh and Segawa references would yield a method that forms a TEOS film over a polysilicon resistor, **after** (instead of before) a resistance value has been provided to the polysilicon resistor by masked implantation of dopant ions into the polysilicon resistor. Further, the masked implantation of dopant ions in such a combination method would be conducted **directly over the polysilicon resistor**, instead of through the TEOS film.

Correspondingly, claims 1-2 and 4-16 of the present application patentably distinguish the combination of the Kadosh and Segawa references, by reciting a method that forms the protective dielectric layer **before** a predetermined resistance value is provided to the polysilicon layer in the at least one polysilicon resistor device region, or by reciting a method that implants ions into polysilicon layer in the polysilicon resistor **through the protective layer**.

Applicants respectfully request the Examiner to reconsider, and upon reconsideration to withdraw, the prior art rejections of claims 1-2 and 4-20.

CONCLUSION

Based on the foregoing, claims 1-2 and 4-20 as amended herein are in condition for allowance. Issue of a Notice of Allowance for the application is therefore requested. If any issues remain outstanding, incident to the formal allowance of the application, the Examiner is requested to contact the undersigned attorney at (516) 742-4343 to discuss same, in order that this application may be allowed and passed to issue at an early date.

Respectfully submitted,

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